

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

- 1 1. (currently amended) A mixer circuit for generating an IF output responsive to an RF input
2 and a LO drive source, comprising:
3 a mixer core having a doubly balanced mixer including a first differentially coupled
4 transistor pair and a second differentially coupled transistor pair;
5 an RF input circuit coupled to the mixer core, the RF input circuit comprising:
6 an ~~input~~ first inductor having a first terminal coupled to receive an RF input signal
7 and a second terminal;
8 a biasing resistor having a first terminal coupled to the second terminal of the
9 ~~input~~ first inductor and a second terminal coupled to a first bias voltage;
10 a first input transistor having a ~~control~~ first terminal coupled to the second
11 terminal of the ~~input~~ first inductor, a second terminal, and a third terminal;
12 a second inductor having a first terminal coupled to the second terminal of the
13 first input transistor and to the first differentially coupled transistor pair,
14 the second inductor also having a second terminal coupled to a ground
15 potential;
16 a supply resistor having a first terminal coupled to the ~~second~~ third terminal of the
17 first input transistor and a second terminal coupled to a supply potential;
18 a first capacitor having a first terminal also coupled to the ~~second~~ third terminal of
19 the first input transistor and a second terminal coupled to the second
20 differentially coupled transistor pair; and
21 a third inductor having a first terminal coupled to the second terminal of the first
22 capacitor and a second terminal coupled to the ground potential.
- 1 2. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled
2 transistor pair, the second differentially coupled transistor pair and the first input
3 transistor are all npn transistors.

- 1 3. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled
2 transistor pair, the second differentially coupled transistor pair and the first input
3 transistor are all pnp transistors.
- 1 4. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled
2 transistor pair, the second differentially coupled transistor pair and the first input
3 transistor are all MOSFET transistors.
- 1 5. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled
2 transistor pair, the second differentially coupled transistor pair and the first input
3 transistor are all MESFET transistors.
- 1 6. (currently amended) A mixer circuit for generating an IF output responsive to an RF input
2 and a LO drive source, comprising:
3 a mixer core having a doubly balanced mixer including a first differentially coupled
4 transistor pair and a second differentially coupled transistor pair, the mixer core
5 coupled to receive a LO drive signal, the LO drive signal having a plurality of
6 harmonics;
7 a low noise RF input circuit coupled to the mixer core through a folded cascode circuit,
8 the low noise RF input circuit coupled to receive an RF input signal, wherein the
9 folded cascode circuit further isolates the low noise RF input circuit from the LO
10 drive signal and the plurality of harmonics.
- 1 7. (currently amended) ~~A~~ The mixer circuit as in Claim 6 wherein the folded cascode circuit
2 comprises:
3 a first cascode transistor having an emitter terminal coupled to a second terminal of a
4 first capacitor and to a first terminal of a ~~third~~ first inductor, a collector terminal
5 coupled to the second differentially coupled transistor pair and a base terminal,
6 a second cascode transistor having a base terminal coupled to the base terminal of the first
7 cascode transistor, an emitter terminal coupled to a first terminal of a second
8 inductor and to an emitter terminal of a first transistor, and a collector terminal
9 coupled to the first differentially coupled transistor pair,

10 a second capacitor, having a first terminal coupled to the emitter terminal of the second
11 cascode transistor and a second terminal coupled to a the second terminal of the
12 first capacitor, the base terminal of the first cascode transistor and to the base
13 terminal of the second cascode transistor,
14 a third capacitor, having a first terminal coupled to the emitter terminal of the first
15 cascode transistor and a second terminal coupled to the second terminal of the
16 second capacitor,
17 a ~~second biasing~~ first resistor having a first terminal coupled to the first terminal of the
18 second capacitor and a second terminal coupled to a second bias voltage.

1 8. (currently amended) ~~A~~ The mixer circuit as in Claim 7, wherein the low noise RF input
2 circuit further includes a RF feedback circuit, the RF feedback circuit comprising:
3 a second transistor having a base terminal coupled to the supply potential, an emitter
4 terminal coupled to ~~the~~ a collector terminal of the first ~~input~~ transistor and a
5 collector terminal coupled to ~~the~~ a first terminal of ~~the~~ a supply resistor and to ~~the~~
6 a first terminal of the first capacitor,
7 a feedback resistor, having a first terminal coupled to ~~the~~ a base terminal of the first ~~input~~
8 transistor and a second terminal,
9 a ~~second~~ fourth capacitor, having a first terminal coupled to the second terminal of the
10 feedback resistor and a second terminal coupled to the first terminal of the supply
11 resistor.

1 9. (currently amended) ~~A~~ The mixer circuit as in Claim 7, wherein the mixer core further
2 includes a tracking supply circuit, the tracking supply circuit comprising:
3 a first diode-connected transistor having a cathode terminal coupled to ~~the~~ a
4 ground potential and an anode terminal,
5 a second diode-connected transistor having a cathode terminal coupled to the
6 anode terminal of the first diode connected transistor and an anode
7 terminal,
8 a ~~third~~ first resistor having a first terminal coupled to the anode terminal of the
9 second diode connected transistor and a second terminal,
10 a first current supply having a first terminal coupled to the second terminal of the
11 ~~third~~ first resistor and a second terminal coupled to the supply potential,

12 a loop amplifier having a first terminal coupled to the second terminal of the ~~third~~
13 first resistor and to the first terminal of the first current supply, a second
14 terminal coupled to the supply potential, a third terminal coupled to the
15 ground potential and a fourth terminal,
16 a ~~fourth~~ second resistor having a first terminal coupled to the fourth terminal of
17 the loop amplifier and a second terminal,
18 a ~~second~~ third transistor having a collector terminal coupled to the second
19 terminal of the ~~fourth~~ second resistor, a base terminal coupled to receive a
20 first LO drive signal and emitter terminal,
21 a ~~third~~ fourth transistor having a base terminal coupled to receive a second LO
22 drive signal, an emitter terminal coupled to the emitter terminal of the
23 second transistor and a collector terminal,
24 a ~~fifth~~ third resistor having a first terminal coupled to the fourth terminal of the
25 loop amplifier and a second terminal coupled to the collector terminal of
26 the third transistor
27 a second current supply having a first terminal coupled to the emitter terminal of
28 the ~~second~~ third transistor and to the emitter terminal of the ~~third~~ fourth
29 transistor and a second terminal coupled to the ground potential,
30 a first common collector amplifier having a base terminal coupled to the second
31 terminal of the ~~fifth~~ third resistor and to the collector terminal of the ~~third~~
32 fourth transistor, a collector terminal coupled to the fourth terminal of the
33 loop amplifier, and an emitter terminal coupled to a first mixer core LO
34 input,
35 a third current supply having a first terminal coupled to the emitter terminal of the
36 first common collector amplifier and a second terminal coupled to the
37 ground potential,
38 a second common collector amplifier having a base terminal coupled to the
39 second terminal of the fourth resistor and to the collector terminal of the
40 second transistor, a collector terminal coupled to the fourth terminal of the
41 loop amplifier and an emitter terminal coupled to a second mixer core LO
42 input,

43 a fourth current supply having a first terminal coupled to the emitter terminal of
44 the second common collector amplifier and a second terminal coupled to
45 the ground potential.

1 10. (currently amended) ~~A~~ The mixer circuit as in Claim 7, wherein the low noise RF input
2 circuit further includes a tracking mixer bias current circuit coupled to the second bias
3 input terminal, the tracking mixer bias current circuit comprising:
4 a ~~third~~ second resistor having a first terminal coupled to the supply potential and a second
5 terminal,
6 a first diode connected transistor having a anode terminal coupled to the second terminal
7 of the ~~third~~ second resistor and a cathode terminal,
8 a second transistor having a collector terminal coupled to the cathode terminal of the first
9 diode connected transistor, an emitter terminal coupled to the ground potential and
10 a base terminal,
11 a loop amplifier having a first terminal coupled to the emitter terminal of the first diode
12 connected transistor and to the collector terminal of the second transistor, a
13 second terminal coupled to the second bias voltage and a third terminal,
14 a ~~fourth~~ third resistor having a first terminal coupled to the base terminal of the second
15 ~~{npn}~~ transistor and a second terminal coupled to the second terminal of the loop
16 amplifier and to the second bias voltage,
17 a bandgap voltage supply having a first terminal coupled to the ground potential and a
18 second terminal coupled to the third terminal of the loop amplifier.

1 11. (currently amended) ~~A~~ The mixer circuit as in Claim 6, wherein the mixer core further
2 includes a tracking supply circuit, the tracking supply circuit comprising:
3 a first diode-connected transistor having a cathode terminal coupled to ~~the~~ a
4 ground potential and an anode terminal,
5 a second diode-connected transistor having a cathode terminal coupled to the
6 anode terminal of the first diode connected transistor and an anode
7 terminal,
8 a ~~third~~ first resistor having a first terminal coupled to the anode terminal of the
9 second diode connected transistor and a second terminal,

10 a first current supply having a first terminal coupled to the second terminal of the
11 ~~third~~ first resistor and a second terminal coupled to the supply potential,
12 a loop amplifier having a first terminal coupled to the second terminal of the ~~third~~
13 first resistor and to the first terminal of the first current supply, a second
14 terminal coupled to the supply potential, a third terminal coupled to the
15 ground potential and a fourth terminal,
16 a ~~fourth~~ second resistor having a first terminal coupled to the fourth terminal of
17 the loop amplifier and a second terminal,
18 a second transistor having a collector terminal coupled to the second terminal of
19 the fourth resistor, a base terminal coupled to receive a first LO drive
20 signal and emitter terminal,
21 a third transistor having a base terminal coupled to receive a second LO drive
22 signal, an emitter terminal coupled to the emitter terminal of the second
23 transistor and a collector terminal,
24 a ~~fifth~~ third resistor having a first terminal coupled to the fourth terminal of the
25 loop amplifier and a second terminal coupled to the collector terminal of
26 the third transistor
27 a second current supply having a first terminal coupled to the emitter terminal of
28 the second transistor and to the emitter terminal of the third transistor and
29 a second terminal coupled to the ground potential,
30 a first common collector amplifier having a base terminal coupled to the second
31 terminal of the ~~fifth~~ third resistor and to the collector terminal of the third
32 transistor, a collector terminal coupled to the fourth terminal of the loop
33 amplifier, and an emitter terminal coupled to a first mixer core LO input,
34 a third current supply having a first terminal coupled to the emitter terminal of the
35 first common collector amplifier and a second terminal coupled to the
36 ground potential,
37 a second common collector amplifier having a base terminal coupled to the
38 second terminal of the ~~fourth~~ second resistor and to the collector terminal
39 of the second transistor, a collector terminal coupled to the fourth terminal
40 of the loop amplifier and an emitter terminal coupled to a second mixer
41 core LO input,

42 a fourth current supply having a first terminal coupled to the emitter terminal of
43 the second common collector amplifier and a second terminal coupled to
44 the ground potential.

1 12. (currently amended) A ~~The~~ mixer circuit as in Claim 6, wherein the low noise RF input
2 circuit further includes a RF feedback circuit coupled to the RF input circuit, the RF
3 feedback circuit comprising:
4 a second transistor having a base terminal coupled to ~~the~~ a supply potential, an
5 emitter terminal coupled to the collector terminal of the first ~~input~~
6 transistor and a collector terminal coupled to ~~the~~ a first terminal of the
7 supply resistor and to ~~the~~ a first terminal of the first capacitor,
8 a feedback resistor, having a first terminal coupled to ~~the~~ a base terminal of the
9 first ~~input~~ transistor and a second terminal,
10 a second capacitor, having a first terminal coupled to the second terminal of the
11 feedback resistor and a second terminal coupled to the first terminal of the
12 supply resistor.

1 13. (currently amended) A quadrature mixer circuit for generating a quadrature IF output
2 responsive to an RF input and a quadrature pair of LO drive signals, comprising:
3 a mixer core having a first doubly balanced mixer including a first differentially
4 coupled transistor pair and a second differentially coupled transistor pair
5 and a second doubly balanced mixer including a third differentially
6 coupled transistor pair and a fourth differentially coupled transistor pair;
7 an RF input circuit coupled to the mixer core, the RF input circuit comprising:
8 an input inductor having a first terminal coupled to receive an RF input signal and
9 a second terminal;
10 a biasing resistor having a first terminal coupled to the second terminal of the
11 input inductor and a second terminal coupled to a first bias voltage;
12 a first input transistor having a base terminal coupled to the second terminal of
13 the input inductor, an emitter terminal, and a collector terminal;
14 a second inductor having a first terminal coupled to the emitter of the first ~~input~~
15 transistor and to the first differentially coupled transistor pair and to the

16 third differentially coupled transistor pair, the second inductor also having
17 a second terminal coupled to a ground potential;
18 a supply resistor having a first terminal coupled to the collector of the first input
19 transistor and a second terminal coupled to a supply potential;
20 a first capacitor having a first terminal also coupled to the collector of the first
21 transistor and a second terminal coupled to the second differentially
22 coupled transistor pair and to the fourth differentially coupled transistor
23 pair; and
24 a third inductor having a first terminal coupled to the second terminal of the first
25 capacitor and a second terminal coupled to the ground potential.

- 1 14. (currently amended) A quadrature mixer circuit for generating a quadrature IF output
2 responsive to an RF input and a quadrature pair of LO drive signals, comprising:
3 a mixer core having a first doubly balanced mixer including a first differentially coupled
4 transistor pair and a second differentially coupled transistor pair and having a
5 second doubly balanced mixer including a third differentially coupled transistor
6 pair and a fourth differentially coupled transistor pair; the mixer core coupled to
7 receive a quadrature LO drive signal, the quadrature LO drive signal having a
8 plurality of harmonics;
9 a low noise RF input circuit coupled to the mixer core through a folded cascode circuit,
10 the low noise RF input circuit coupled to receive an RF input signal, wherein the
11 folded cascode circuit further isolates the low noise RF input circuit from the
12 quadrature LO drive signal and the plurality of harmonics,
13 a first cascode capacitor, a first terminal of the first cascode capacitor coupled to ~~the~~ an
14 emitter terminal of a first cascode transistor and a second node of the first cascode
15 capacitor coupled to ~~the~~ base terminals of the first cascode transistor and a second
16 cascode transistor,
17 a second cascode capacitor, a first terminal of the second cascode capacitor coupled to the
18 base terminals of the first cascode transistor and the second cascode transistor and
19 ~~the~~ a second node of the second cascode capacitor coupled to ~~the~~ an emitter
20 terminal of the second cascode transistor.
21

- 1 15. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 14 wherein the folded
2 cascode circuit comprises:
3 a first cascode transistor having an emitter terminal coupled to ~~the~~ a second terminal of
4 ~~the~~ a first capacitor and to ~~the~~ a first terminal of ~~the third~~ a first inductor, a
5 collector terminal coupled to the second differentially coupled transistor pair and a
6 base terminal,
7 a second cascode transistor having a base terminal coupled to the base terminal of the first
8 cascode transistor, an emitter terminal coupled to ~~the~~ a first terminal of ~~the~~ a
9 second inductor and to the emitter terminal of the first transistor and a collector
10 terminal coupled to the first differentially coupled transistor pair,
11 ~~a second capacitor, having a first terminal coupled to the collector terminal of the first~~
12 ~~cascode transistor and a second terminal coupled to the base terminal of the first~~
13 ~~cascode transistor and to the base terminal of the second cascode transistor,~~
14 ~~a third capacitor, having a first terminal coupled to the emitter terminal of the second~~
15 ~~cascode transistor and a second terminal coupled to the second terminal of the~~
16 ~~second capacitor and to the base terminal of the first cascode transistor and to the~~
17 ~~base terminal of the first second cascode transistor,~~
18 a second biasing first resistor having a first terminal coupled to the second terminal of the
19 second first cascode capacitor and the first terminal of the ~~third~~ first cascode
20 capacitor and a second terminal coupled to a second first bias voltage,
21 a ~~third biasing second~~ resistor having a first terminal coupled to the ~~second first~~ bias
22 voltage and to the second terminal of the second biasing first resistor and having a
23 second terminal,
24 a third cascode transistor having a collector terminal coupled to the fourth differentially
25 coupled transistor pair, an emitter terminal coupled to the ~~second first~~ terminal of
26 the ~~third first~~ inductor and to the emitter terminal of the first cascode transistor,
27 and a base terminal,
28 a fourth cascode transistor having a base terminal coupled to the base terminal of the third
29 cascode transistor, a collector terminal coupled the third differentially coupled
30 transistor pair and an emitter terminal coupled to the emitter terminal of the
31 second cascode transistor and to the second first terminal of the second inductor,

32 a ~~fourth~~ third cascode capacitor having a first terminal coupled to the emitter terminal of
33 the third cascode transistor and a second terminal coupled to the base terminal of
34 the third and fourth cascode transistors,
35 a ~~fifth~~ fourth cascode capacitor having a first terminal coupled to the second terminal of
36 the ~~fourth~~ third cascode capacitor and to the base terminals of the third and fourth
37 cascode transistors and a second terminal coupled to the emitter terminal of the
38 fourth cascode transistor.

1 16. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 15 wherein the low
2 noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit
3 comprising:
4 a second transistor having a base terminal coupled to ~~the~~ a supply potential, an
5 emitter terminal coupled to the collector terminal of the first ~~input~~
6 transistor and a collector terminal coupled to ~~the~~ a first terminal of the
7 supply resistor and to ~~the~~ a first terminal of the first capacitor,
8 a feedback resistor, having a first terminal coupled to ~~the~~ a base terminal of the
9 first input transistor and a second terminal,
10 a ~~sixth~~ second capacitor, having a first terminal coupled to the second terminal of
11 the feedback resistor and a second terminal coupled to the first terminal of
12 the supply resistor.

1 17. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 16, wherein the mixer
2 core further includes a first tracking supply circuit portion coupled to ~~the~~ In-Phase LO
3 drive input terminals of the mixer core and a second tracking supply circuit portion
4 coupled to ~~the~~ Quadrature Phase LO drive input terminals of the mixer core.

1 18. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 17, wherein the first
2 tracking supply circuit portion comprises:
3 a. a first diode-connected transistor having a cathode terminal coupled to ~~the~~ a
4 ground potential and an anode terminal;
5 b. a second diode-connected transistor having a cathode terminal coupled to the
6 anode terminal of the first diode connected transistor and an anode terminal,

- c. a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;
- d. a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential;
- e. a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;
- f. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;
- g. a ~~second~~ third transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and an emitter terminal;
- h. a third ~~fourth~~ transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the ~~second~~ third transistor and a collector terminal;
- i. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the ~~third~~ fourth transistor;
- j. a second current supply having a first terminal coupled to the emitter terminal of the ~~second~~ third transistor and to the emitter terminal of the ~~third~~ fourth transistor and a second terminal coupled to the ground potential;
- k. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the ~~third~~ fourth transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;
- l. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;
- m. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the ~~second~~ third transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input; and

- 40 n. a fourth current supply having a first terminal coupled to the emitter terminal of
41 the second common collector amplifier and a second terminal coupled to the
42 ground potential;
- 43 and wherein the second tracking supply circuit portion comprises:
- 44 o. a third diode-connected transistor having a cathode terminal coupled to the ground
45 potential and an anode terminal;
- 46 p. a fourth diode-connected transistor having a cathode terminal coupled to the
47 anode terminal of the third diode connected transistor and an anode terminal;
- 48 q. a ~~third~~ sixth resistor having a first terminal coupled to the anode terminal of the
49 second diode connected transistor and a second terminal;
- 50 r. a ~~first~~ fifth current supply having a first terminal coupled to the second terminal of
51 the ~~third~~ sixth resistor and a second terminal coupled to the supply potential;
- 52 s. a second loop amplifier having a first terminal coupled to the second terminal of
53 the ~~third~~ sixth resistor and to the first terminal of the ~~first~~ fifth current supply, a
54 second terminal coupled to the supply potential, a third terminal coupled to the
55 ground potential and a fourth terminal;
- 56 t. a ~~fourth~~ seventh resistor having a first terminal coupled to the fourth terminal of
57 the second loop amplifier and a second terminal;
- 58 u. a ~~second~~ fourth transistor having a collector terminal coupled to the second
59 terminal of the ~~fourth~~ seventh resistor, a base terminal coupled to receive a first
60 LO drive signal and emitter terminal;
- 61 v. a ~~third~~ fourth transistor having a base terminal coupled to receive a second LO
62 drive signal, an emitter terminal coupled to the emitter terminal of the ~~second~~
63 fourth transistor and a collector terminal;
- 64 w. a ~~fifth~~ eighth resistor having a first terminal coupled to the fourth terminal of the
65 second loop amplifier and a second terminal coupled to the collector terminal of
66 the ~~third~~ fourth transistor;
- 67 x. a ~~second~~ sixth current supply having a first terminal coupled to the emitter
68 terminal of the ~~second~~ fourth transistor and to the emitter terminal of the ~~third~~
69 fourth transistor and a second terminal coupled to the ground potential;
- 70 y. a ~~first~~ third common collector amplifier having a base terminal coupled to the
71 second terminal of the ~~fifth~~ eighth resistor and to the collector terminal of the ~~third~~

72 fourth transistor, a collector terminal coupled to the fourth terminal of the second
73 loop amplifier, and an emitter terminal coupled to a first mixer core LO input;
74 z. a ~~third~~ seventh current supply having a first terminal coupled to the emitter
75 terminal of the ~~first~~ third common collector amplifier and a second terminal
76 coupled to the ground potential;
77 aa. a ~~second~~ fourth common collector amplifier having a base terminal coupled to the
78 second terminal of the ~~fourth~~ seventh resistor and to the collector terminal of the
79 ~~second~~ fourth transistor, a collector terminal coupled to the fourth terminal of the
80 second loop amplifier and an emitter terminal coupled to a second mixer core LO
81 input;
82 ab. a ~~fourth~~ eighth current supply having a first terminal coupled to the emitter
83 terminal of the ~~second~~ fourth common collector amplifier and a second terminal
84 coupled to the ground potential.

1 19. (currently amended) A The quadrature mixer circuit as in Claim 15, wherein the low
2 noise RF input circuit further includes a tracking mixer bias current circuit, the tracking
3 bias current circuit comprising:
4 a first resistor having a first terminal coupled to the supply potential and a second
5 terminal,
6 a first diode connected transistor having a anode terminal coupled to the second
7 terminal of the third resistor and a cathode terminal,
8 a second transistor having a collector terminal coupled to the cathode terminal of
9 the first diode connected transistor, an emitter terminal coupled to the
10 ground potential and a base terminal,
11 a loop amplifier having a first terminal coupled to the emitter terminal of the first
12 diode connected transistor and to the collector terminal of the second
13 transistor, a second terminal coupled to the ~~second~~ first bias voltage and a
14 third terminal,
15 a second resistor having a first terminal coupled to the base terminal of the second
16 transistor and a second terminal coupled to the second terminal of the loop
17 amplifier and to the ~~second~~ first bias voltage,
18 a bandgap voltage supply having a first terminal coupled to the ground potential
19 and a second terminal coupled to the third terminal of the loop amplifier.

- 1 20. (canceled)
- 1 21. (currently amended) A mixer circuit for generating an IF output responsive to an RF input
2 and a LO drive source, comprising:
3 a mixer core having a doubly balanced mixer including a first differentially coupled
4 transistor pair and a second differentially coupled transistor pair, the mixer core
5 coupled to receive a LO drive signal, the LO drive signal having a plurality of
6 harmonics;
7 a low noise single ended RF input circuit coupled to the mixer core through a cascode
8 circuit, the low noise single ended RF input circuit coupled to receive an RF input
9 signal, wherein the cascode circuit further isolates the low noise single ended RF
10 input circuit from the LO drive signal and the plurality of harmonics, the low
11 noise single ended RF circuit including means for providing an input impedance
12 and means for splitting a phase of the RF input signal.
- 1 22. (currently amended) The mixer circuit according to Claim 6 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair and
3 the first ~~input~~ transistor are all npn transistors.
- 1 23. (currently amended) The mixer circuit according to Claim 6 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair and
3 the first ~~input~~ transistor are all pnp transistors.
- 1 24. (currently amended) The mixer circuit according to Claim 6 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair and
3 the first ~~input~~ transistor are all MOSFET transistors.
- 1 25. (currently amended) The mixer circuit according to Claim 6 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair and
3 the first ~~input~~ transistor are all MESFET transistors.

- 1 26. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first input transistor are all npn transistors.
- 1 27. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first input transistor are all pnp transistors.
- 1 28. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first input transistor are all MOSFET transistors.
- 1 29. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first input transistor are all MESFET transistors.
- 1 30. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first ~~input~~ transistor are all npn transistors.
- 1 31. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first ~~input~~ transistor are all pnp transistors.
- 1 32. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the

3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first ~~input~~ transistor are all MOSFET transistors.

1 33. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first
2 differentially coupled transistor pair, the second differentially coupled transistor pair, the
3 third differentially coupled transistor pair, the fourth differentially coupled transistor pair
4 and the first ~~input~~ transistor are all MESFET transistors.

1 34. (canceled)

1 35. (canceled)

1 36. (canceled)

1 37. (canceled)

1 38. (currently amended) The mixer circuit according to Claim 21 wherein the first
2 differentially coupled transistor pair[,] and the second differentially coupled transistor
3 pair ~~and the first input transistor~~ are all npn transistors.

1 39. (currently amended) The mixer circuit according to Claim 21 wherein the first
2 differentially coupled transistor pair[,] and the second differentially coupled transistor
3 pair ~~and the first input transistor~~ are all pnp transistors.

1 40. (currently amended) The mixer circuit according to Claim 21 wherein the first
2 differentially coupled transistor pair[,] and the second differentially coupled transistor
3 pair ~~and the first input transistor~~ are all MOSFET transistors.

1 41. (currently amended) The mixer circuit according to Claim 21 wherein the first
2 differentially coupled transistor pair[,] and the second differentially coupled transistor
3 pair ~~and the first input transistor~~ are all MESFET transistors.